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are examined,
with a view to
better defining
the likely
capabilities of
future
microelectronic
systems. This
analysis covers
both data
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processing
applications
such as RF and
imaging.

Finally, we
speculate on the
future of CMOS
for the coming
15-20 years.

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semiconductor
(CMOS)

technologies are
scaled down into
the nanometer
range, a number
of major
nonidealities

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must be
addressed and
overcome to
achieve a
successful
analog and
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analyze the achievable performance and possible limits of CMOS technology from the point of view of device physics, device technology, and power consumption.

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Nanotechnology promises to open up new ways of scaling CMOS circuits by introducing new materials. For example, a hybrid circuit of CMOS gates and carbon nanotubes (CNT),

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extending the performance of electronics systems. In particular, this review introduces and summarizes progress in the development of the tunnel field-effect transistors (TFETs)

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including its
origin, current
experimental and
theoretical
performance
relative to the
metal-oxide-
semiconductor
field ...

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Tunnel
Transistors for
Beyond CMOS**

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ABSTRACT CMOS technology scaling has followed Moore's law well into the nano-scale regime now. The technology scaling is no longer just about geometric reduction but more about

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innovation in
the use of new
materials and
transistor
architectures.

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examined, with a
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likely

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dominance for
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or so despite
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resulting from
the continuous
reduction of
transistor
dimensions.

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All issues . . .

Abstract: As complementary metal-oxide-semiconductor (CMOS) technologies are scaled down into the nanometer range, a number of major nonidealities must be addressed and

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Overcome to
achieve a
successful
analog and
physical circuit
design. The
nature of these
nonidealities
has been well
reported in the
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